(12) UK Patent Application (19) GB (11) 2 289 199 (13) A

(43) Date of A Publication 08.11.1995

(21) Application No 9501802.4

(22) Date of Filing 30.01.1995

(30) Priority Data
(31) 06009757 (32) 31.01.1994 (33) JP

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(51) INT CL[6]
G06T 1/60 1/20

(52) UK CL (Edition N)
H4T TBAD TBEC

(56) Documents Cited
GB 2264616 A GB 2257599 A GB 2208095 A
US 5239512 A US 4912771 A

(58) Field of Search
UK CL (Edition N) H4F FESA FESG FESK FESX, H4T TBAD TCGA TCGD TCGG TCGK TCGX
INT CL[6] G06T 1/60
Online: WPI

(54) Image processing system

(57) An image processing system which updates and displays on a display unit at a high speed the image data stored in an image memory of an address multiplex mode, which system is provided with two multiple-bank image memories (10, 11) each having one picture's worth of capacity, assigns the same row address to each rectangular region of the image data, is provided with two memory control units (12, 13) having address conversion means (18) for converting the X-Y addresses of the image data to addresses of the image memories, switches the image memories in units of pictures so that one control unit writes image data in one image memory and the other control unit reads image data from the other image memory, and is provided with a selection means (14) for selecting either of display image data output from the image memories and sending the same to the display unit.

Fig.1

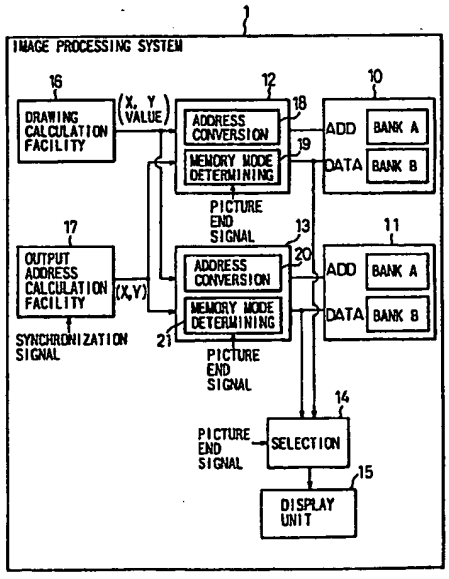

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Fig.1

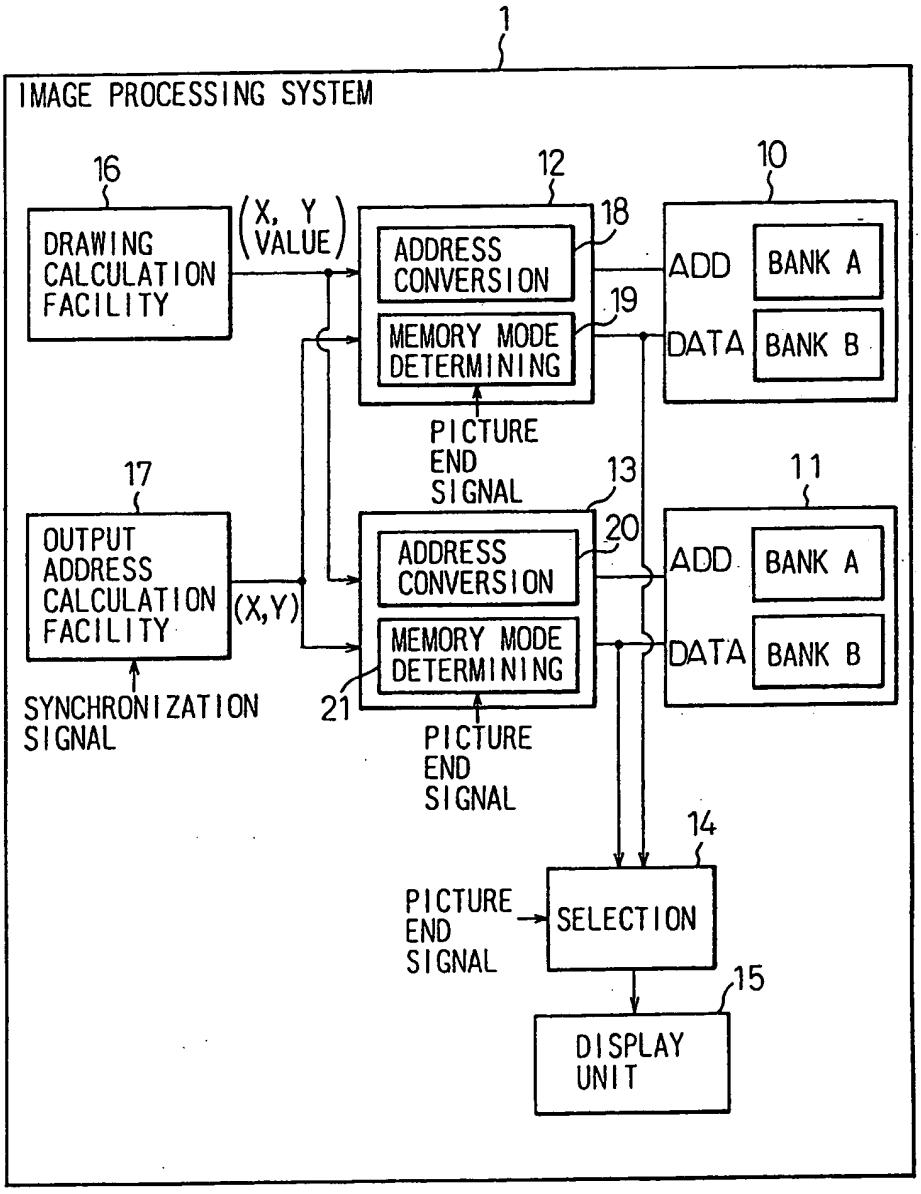

1
IMAGE PROCESSING SYSTEM
16
DRAWING CALCULATION FACILITY
(X, Y VALUE)
12
18
ADDRESS CONVERSION
19
MEMORY MODE DETERMINING
10
ADD
BANK A
DATA
BANK B
PICTURE END SIGNAL
17
OUTPUT ADDRESS CALCULATION FACILITY
(X,Y)
13
20
ADDRESS CONVERSION
MEMORY MODE DETERMINING
21
11
ADD
BANK A
DATA
BANK B
SYNCHRONIZATION SIGNAL
PICTURE END SIGNAL
14
PICTURE END SIGNAL
SELECTION
15
DISPLAY UNIT

Fig. 2

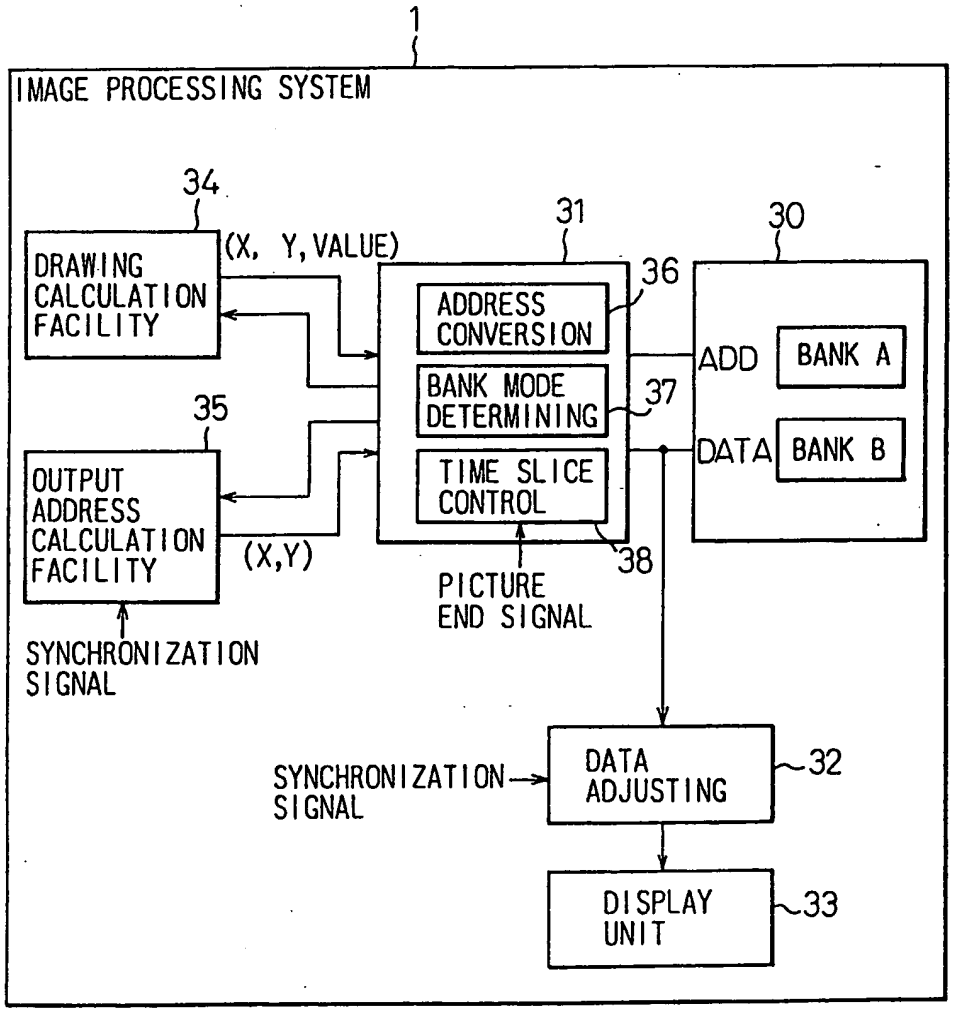

1
IMAGE PROCESSING SYSTEM
34
DRAWING CALCULATION FACILITY
(X, Y, VALUE)
31
30
36
ADDRESS CONVERSION
ADD
BANK A
BANK MODE DETERMINING
37
DATA
BANK B
35
OUTPUT ADDRESS CALCULATION FACILITY
TIME SLICE CONTROL
(X,Y)
38
PICTURE END SIGNAL
SYNCHRONIZATION SIGNAL
SYNCHRONIZATION SIGNAL
DATA ADJUSTING
32
DISPLAY UNIT
33

Fig.3

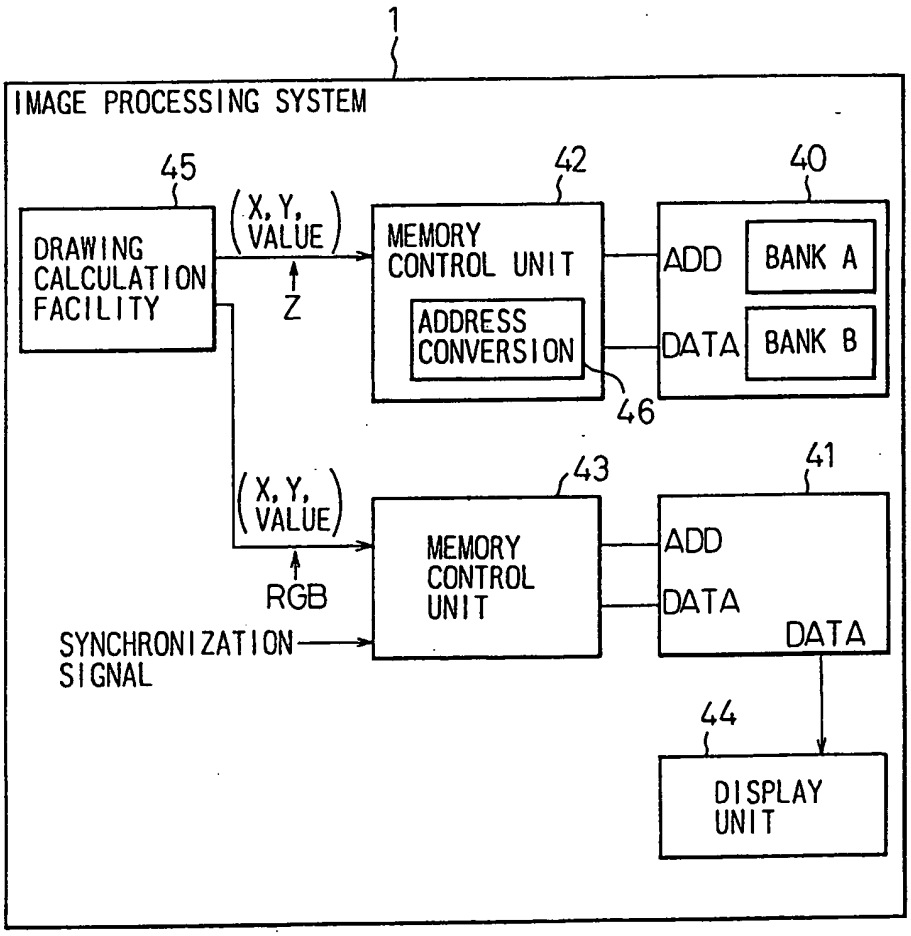

1
IMAGE PROCESSING SYSTEM
45
DRAWING CALCULATION FACILITY
(X, Y, VALUE)
Z
42
MEMORY CONTROL UNIT
ADDRESS CONVERSION
46
40
ADD
BANK A
DATA
BANK B
(X, Y, VALUE)
RGB
43
MEMORY CONTROL UNIT
SYNCHRONIZATION SIGNAL
41
ADD
DATA
DATA
44
DISPLAY UNIT

Fig.4A

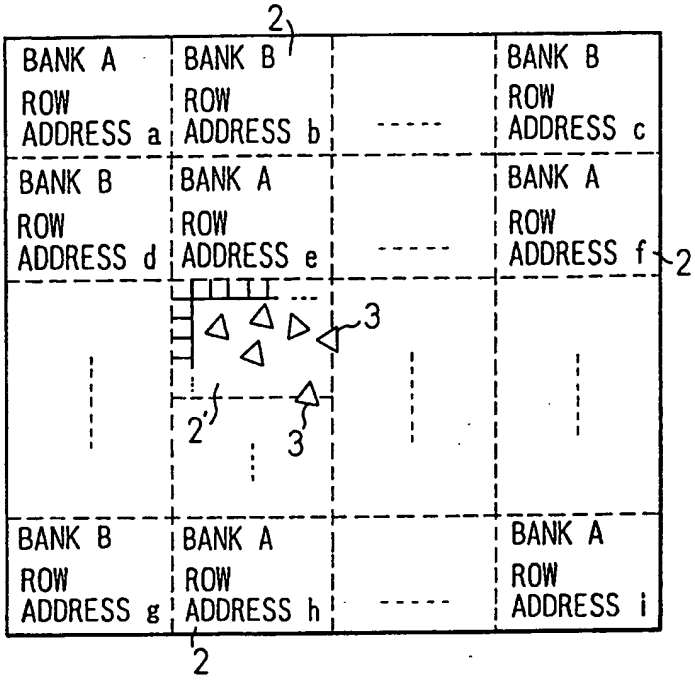

2
BANK A ROW ADDRESS a
BANK B ROW ADDRESS b
BANK B ROW ADDRESS c
BANK B ROW ADDRESS d
BANK A ROW ADDRESS e
BANK A ROW ADDRESS f
2
3
2'
3
BANK B ROW ADDRESS g
BANK A ROW ADDRESS h
BANK A ROW ADDRESS i
2

Fig.4B

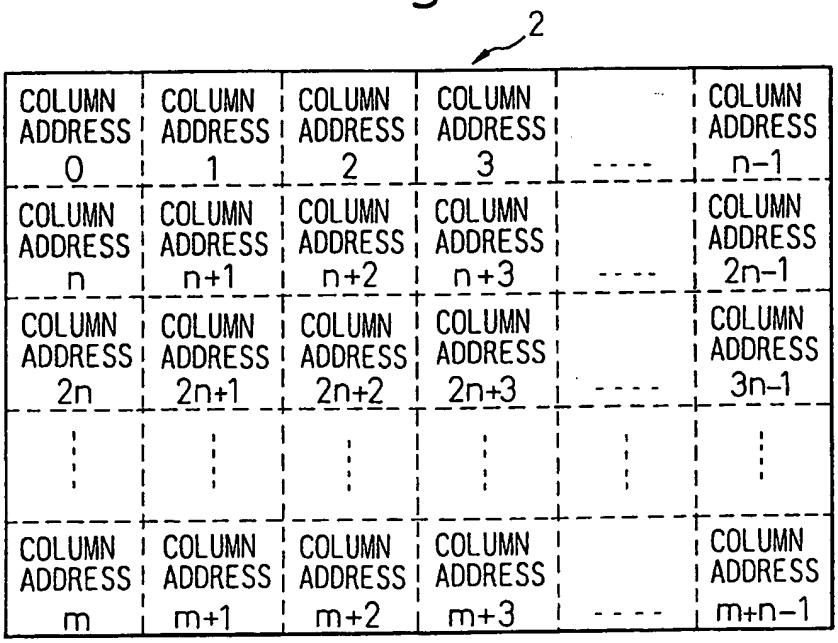

2
COLUMN ADDRESS 0
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS 3
COLUMN ADDRESS n-1
COLUMN ADDRESS n
COLUMN ADDRESS n+1
COLUMN ADDRESS n+2
COLUMN ADDRESS n+3
COLUMN ADDRESS 2n-1
COLUMN ADDRESS 2n
COLUMN ADDRESS 2n+1
COLUMN ADDRESS 2n+2
COLUMN ADDRESS 2n+3
COLUMN ADDRESS 3n-1
COLUMN ADDRESS m
COLUMN ADDRESS m+1
COLUMN ADDRESS m+2
COLUMN ADDRESS m+3
COLUMN ADDRESS m+n-1

Fig.5

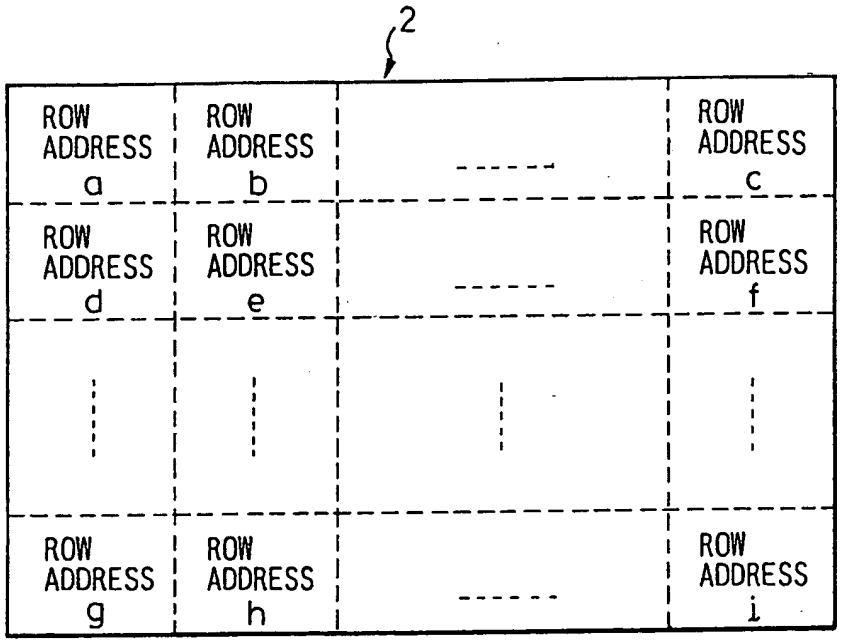

2
ROW ADDRESS a
ROW ADDRESS b
ROW ADDRESS c
ROW ADDRESS d
ROW ADDRESS e
ROW ADDRESS f
ROW ADDRESS g
ROW ADDRESS h
ROW ADDRESS i

Fig.6A

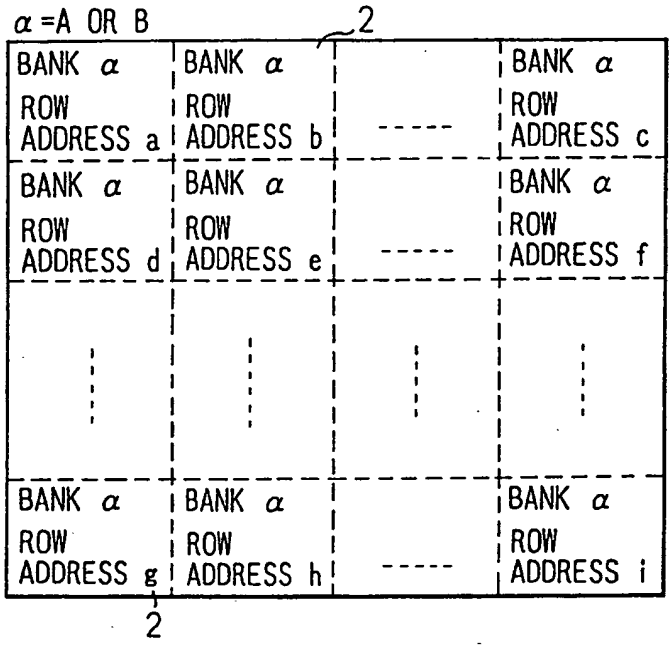

α=A OR B
2
BANK α ROW ADDRESS a
BANK α ROW ADDRESS b
BANK α ROW ADDRESS c
BANK α ROW ADDRESS d
BANK α ROW ADDRESS e
BANK α ROW ADDRESS f
BANK α ROW ADDRESS g
BANK α ROW ADDRESS h
BANK α ROW ADDRESS i
2

Fig.6B

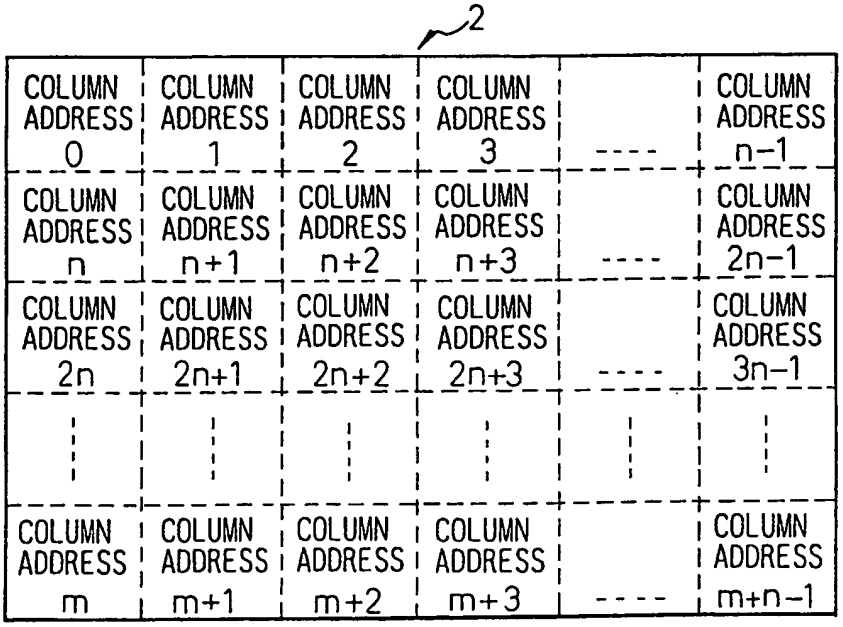
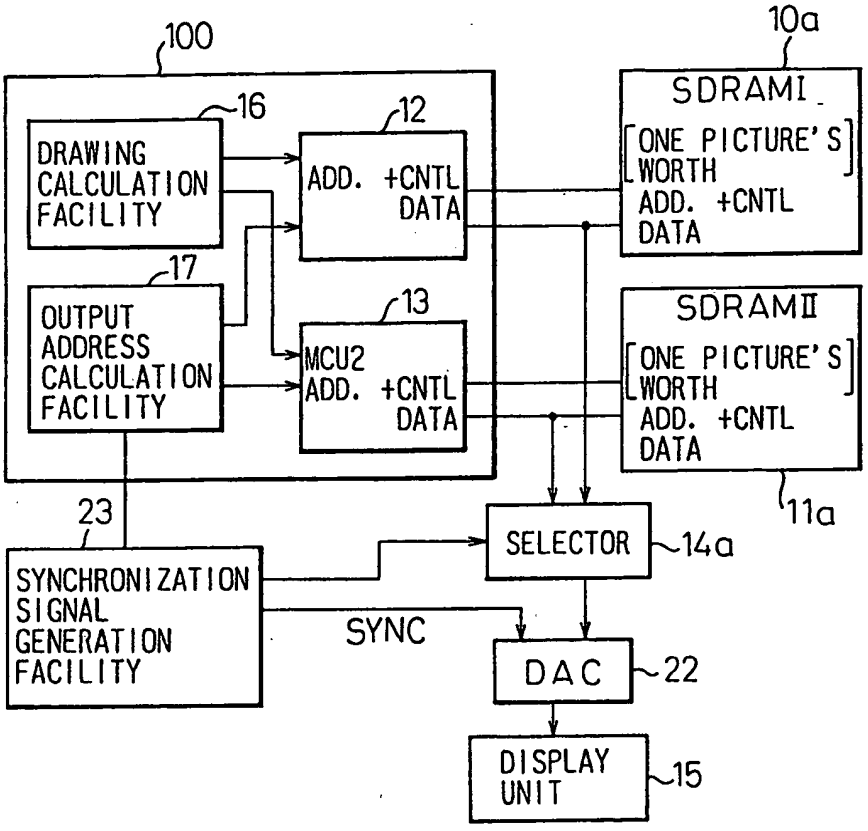

2
COLUMN ADDRESS 0
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS 3
COLUMN ADDRESS n-1
COLUMN ADDRESS n
COLUMN ADDRESS n+1
COLUMN ADDRESS n+2
COLUMN ADDRESS n+3
COLUMN ADDRESS 2n-1
COLUMN ADDRESS 2n
COLUMN ADDRESS 2n+1
COLUMN ADDRESS 2n+2
COLUMN ADDRESS 2n+3
COLUMN ADDRESS 3n-1
COLUMN ADDRESS m
COLUMN ADDRESS m+1
COLUMN ADDRESS m+2
COLUMN ADDRESS m+3
COLUMN ADDRESS m+n-1

Fig.7


100
10a
SDRAMI
[ONE PICTURE'S WORTH ADD. +CNTL DATA]
16
DRAWING CALCULATION FACILITY
12
ADD. +CNTL DATA
17
OUTPUT ADDRESS CALCULATION FACILITY
13
MCU2 ADD. +CNTL DATA
SDRAMII
[ONE PICTURE'S WORTH ADD. +CNTL DATA]
11a
23
SYNCHRONIZATION SIGNAL GENERATION FACILITY
SELECTOR
14a
SYNC
DAC
22
DISPLAY UNIT
15

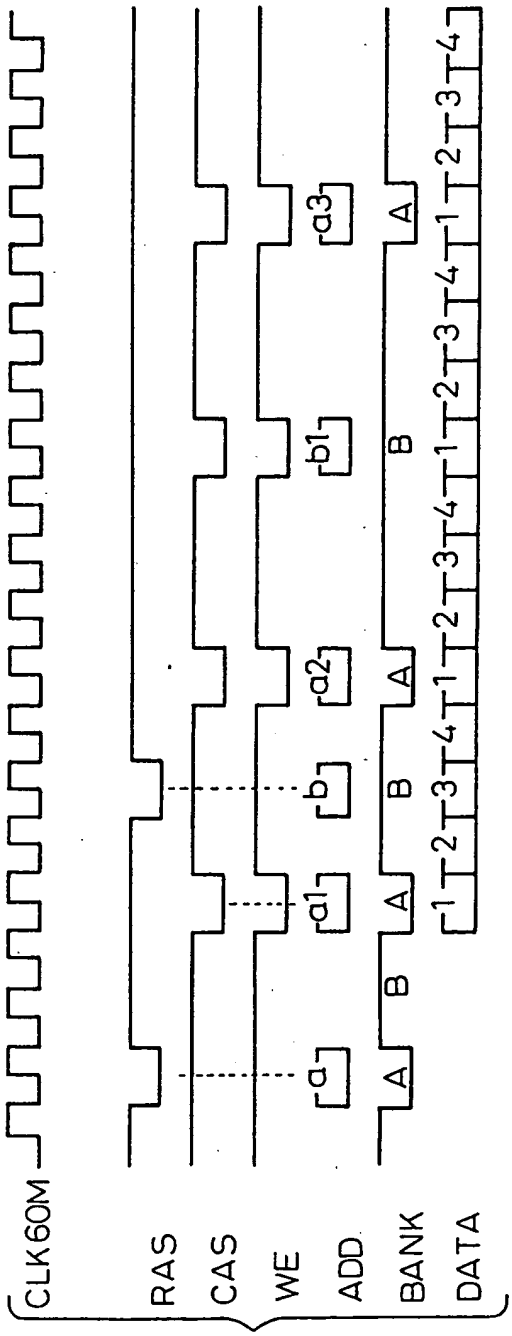

CLK60M
RAS
CAS
WE
ADD
BANK
DATA
a
b
a1
b
a2
b1
a3
A
B
A
B
A
B
A
1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4

Fig.8

Fig.9A

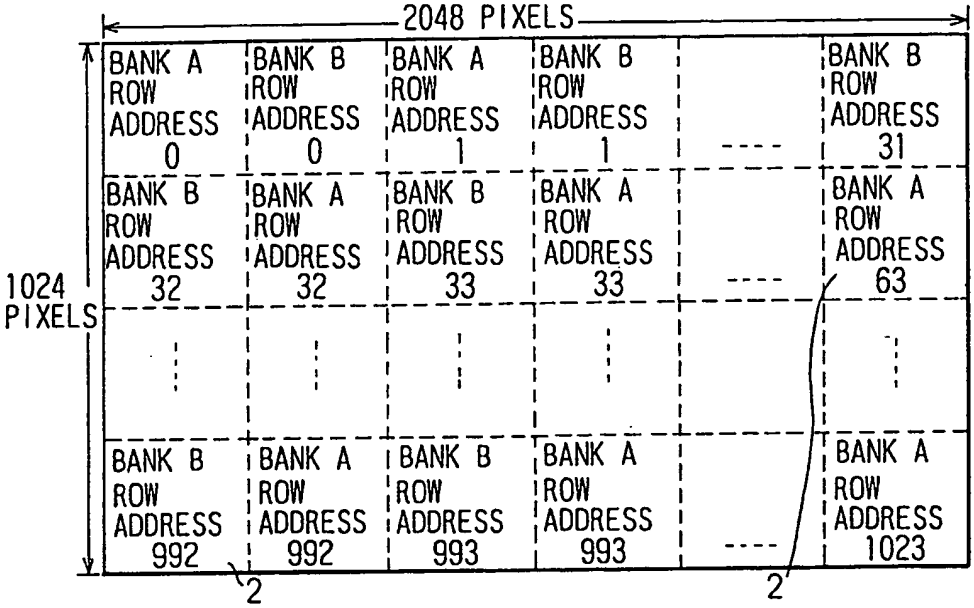

2048 PIXELS
1024 PIXELS
BANK A ROW ADDRESS 0
BANK B ROW ADDRESS 0
BANK A ROW ADDRESS 1
BANK B ROW ADDRESS 1
BANK B ROW ADDRESS 31
BANK B ROW ADDRESS 32
BANK A ROW ADDRESS 32
BANK B ROW ADDRESS 33
BANK A ROW ADDRESS 33
BANK A ROW ADDRESS 63
BANK B ROW ADDRESS 992
BANK A ROW ADDRESS 992
BANK B ROW ADDRESS 993
BANK A ROW ADDRESS 993
BANK A ROW ADDRESS 1023
2
2

Fig.9B

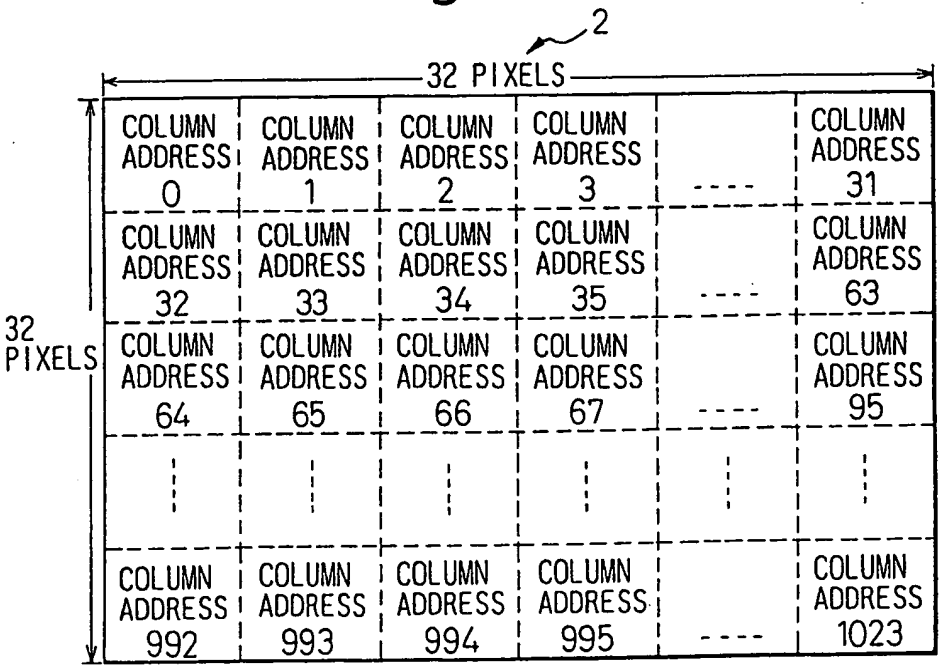

2
32 PIXELS
32 PIXELS
COLUMN ADDRESS 0
COLUMN ADDRESS 1
COLUMN ADDRESS 2
COLUMN ADDRESS 3
COLUMN ADDRESS 31
COLUMN ADDRESS 32
COLUMN ADDRESS 33
COLUMN ADDRESS 34
COLUMN ADDRESS 35
COLUMN ADDRESS 63
COLUMN ADDRESS 64
COLUMN ADDRESS 65
COLUMN ADDRESS 66
COLUMN ADDRESS 67
COLUMN ADDRESS 95
COLUMN ADDRESS 992
COLUMN ADDRESS 993
COLUMN ADDRESS 994
COLUMN ADDRESS 995
COLUMN ADDRESS 1023

Fig.10

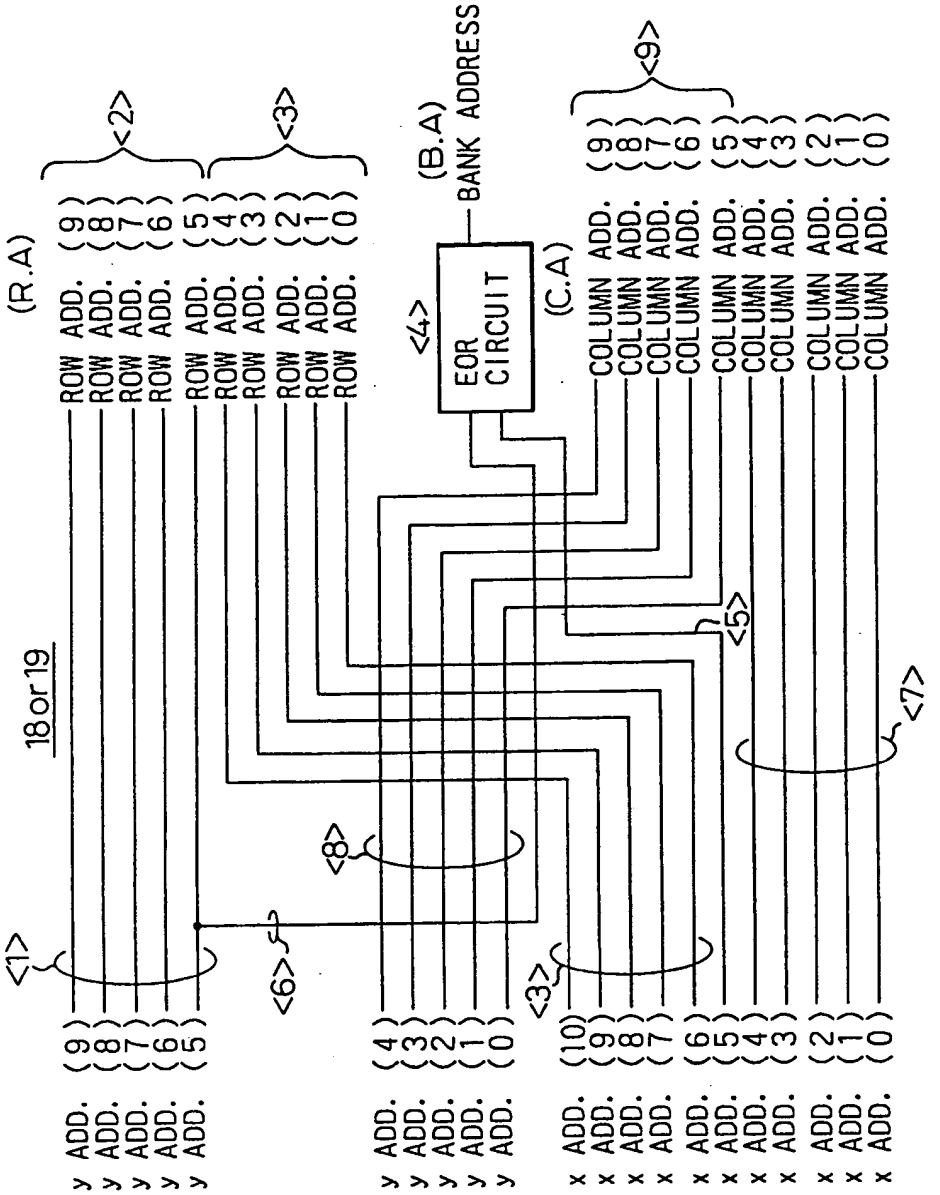

18or19
(R.A)
ROW ADD. (9)
ROW ADD. (8)
ROW ADD. (7)
ROW ADD. (6)
ROW ADD. (5)
ROW ADD. (4)
ROW ADD. (3)
ROW ADD. (2)
ROW ADD. (1)
ROW ADD. (0)
<2>
<3>
(B.A)
BANK ADDRESS
<4>
EOR CIRCUIT
(C.A)
COLUMN ADD. (9)
COLUMN ADD. (8)
COLUMN ADD. (7)
COLUMN ADD. (6)
COLUMN ADD. (5)
COLUMN ADD. (4)
COLUMN ADD. (3)
COLUMN ADD. (2)
COLUMN ADD. (1)
COLUMN ADD. (0)
<9>
<1>
<6>
<8>
<5>
<7>
y ADD. (9)
y ADD. (8)
y ADD. (7)
y ADD. (6)
y ADD. (5)
y ADD. (4)
y ADD. (3)
y ADD. (2)
y ADD. (1)
y ADD. (0)
x ADD. (10)
x ADD. (9)
x ADD. (8)
x ADD. (7)
x ADD. (6)
x ADD. (5)
x ADD. (4)
x ADD. (3)
x ADD. (2)
x ADD. (1)
x ADD. (0)

Fig.11

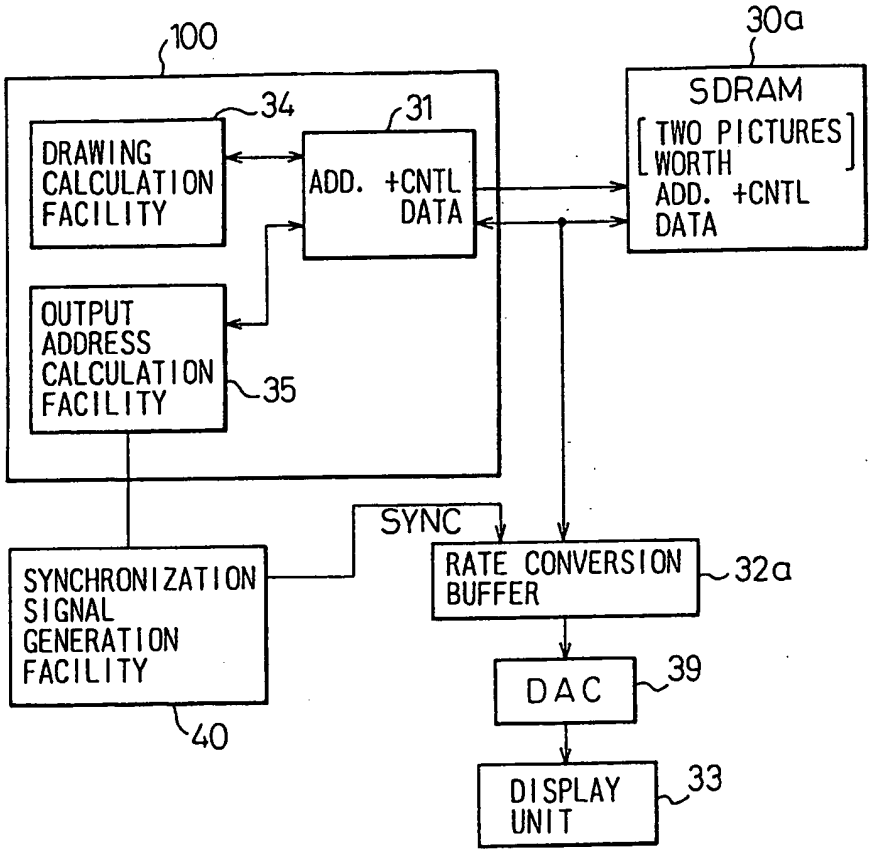

100
30a
SDRAM
[TWO PICTURES WORTH
ADD. +CNTL DATA]
34
31
DRAWING CALCULATION FACILITY
ADD. +CNTL DATA
OUTPUT ADDRESS CALCULATION FACILITY
35
SYNC
SYNCHRONIZATION SIGNAL GENERATION FACILITY
40
RATE CONVERSION BUFFER
32a
DAC
39
DISPLAY UNIT
33

Fig.12A

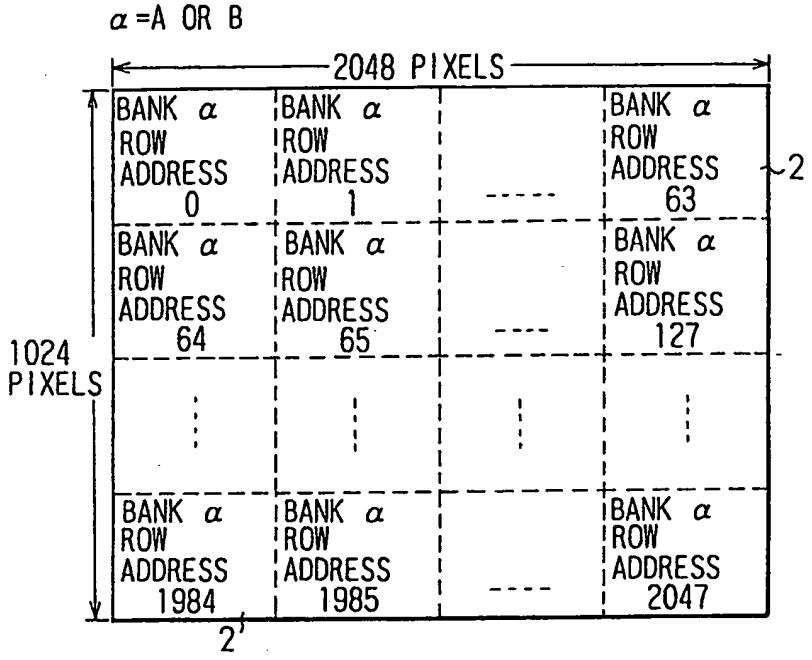


Fig.12B

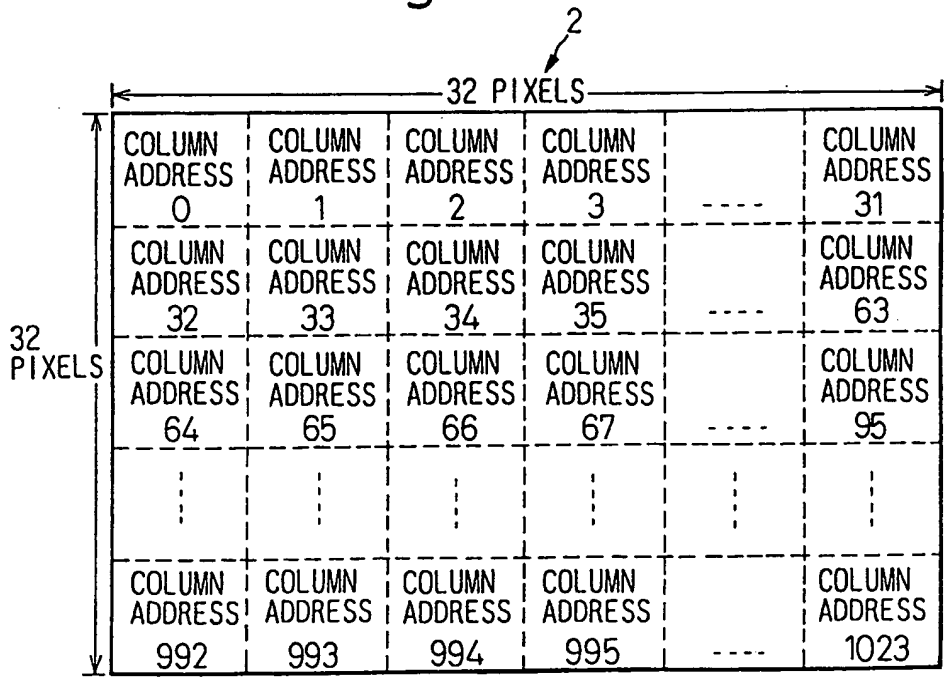


Fig.13

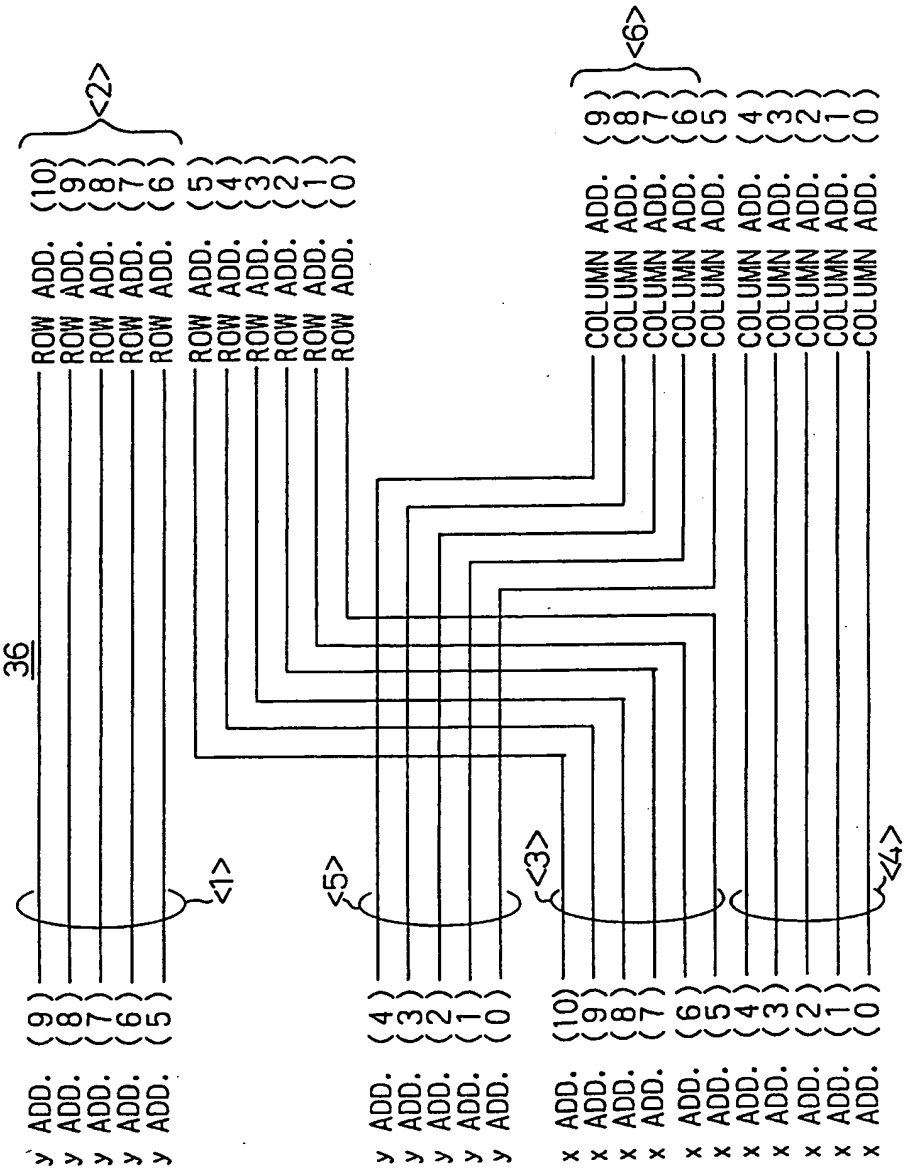

36
y ADD. (9) (8) (7) (6) (5)
y ADD. (4) (3) (2) (1) (0)
x ADD. (10) (9) (8) (7) (6) (5) (4) (3) (2) (1) (0)
<1>
<2>
<3>
<4>
<5>
<6>
ROW ADD. (10) (9) (8) (7) (6)
ROW ADD. (5) (4) (3) (2) (1) (0)
COLUMN ADD. (9) (8) (7) (6) (5) (4) (3) (2) (1) (0)

Fig.14

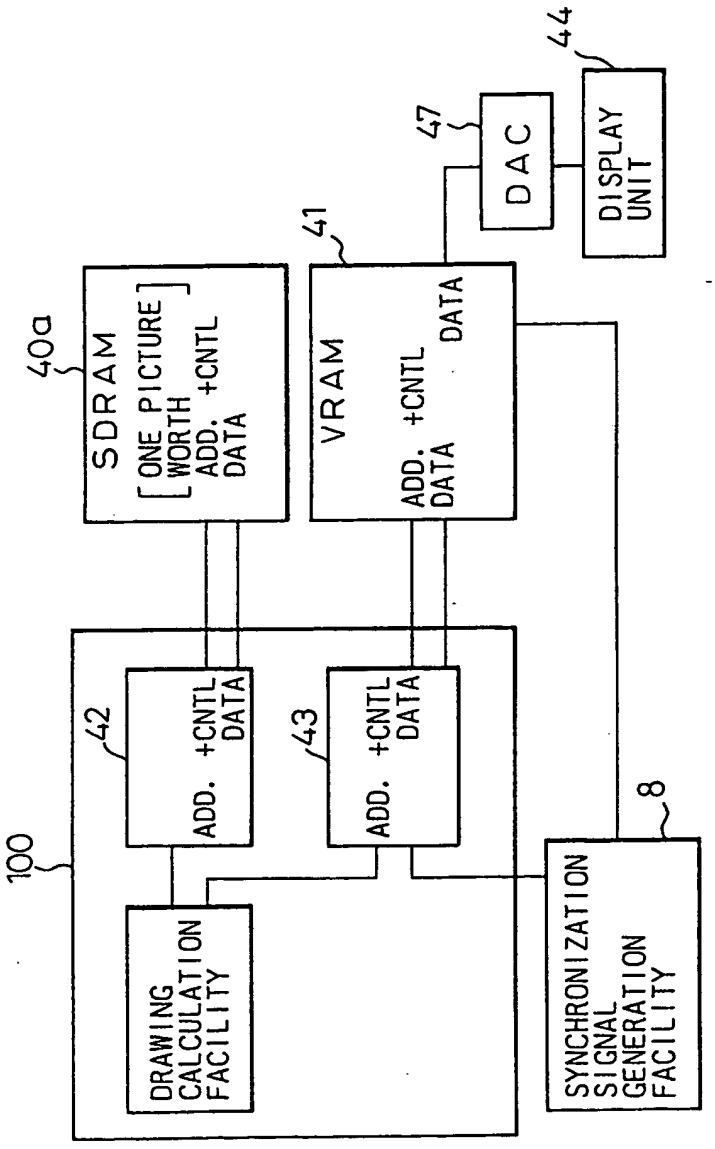

40a
SDRAM
[ONE PICTURE WORTH ADD. DATA +CNTL
41
VRAM
ADD. +CNTL
DATA
47
DAC
44
DISPLAY UNIT
100
42
ADD. +CNTL DATA
43
ADD. +CNTL DATA
DRAWING CALCULATION FACILITY
8
SYNCHRONIZATION SIGNAL GENERATION FACILITY

Fig.15

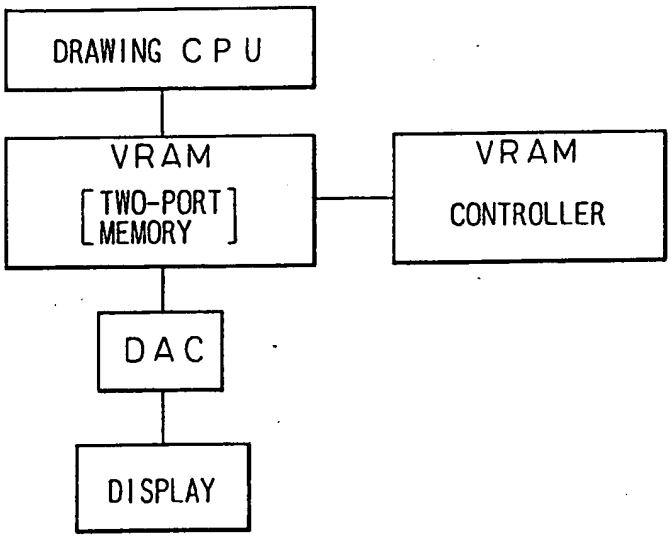
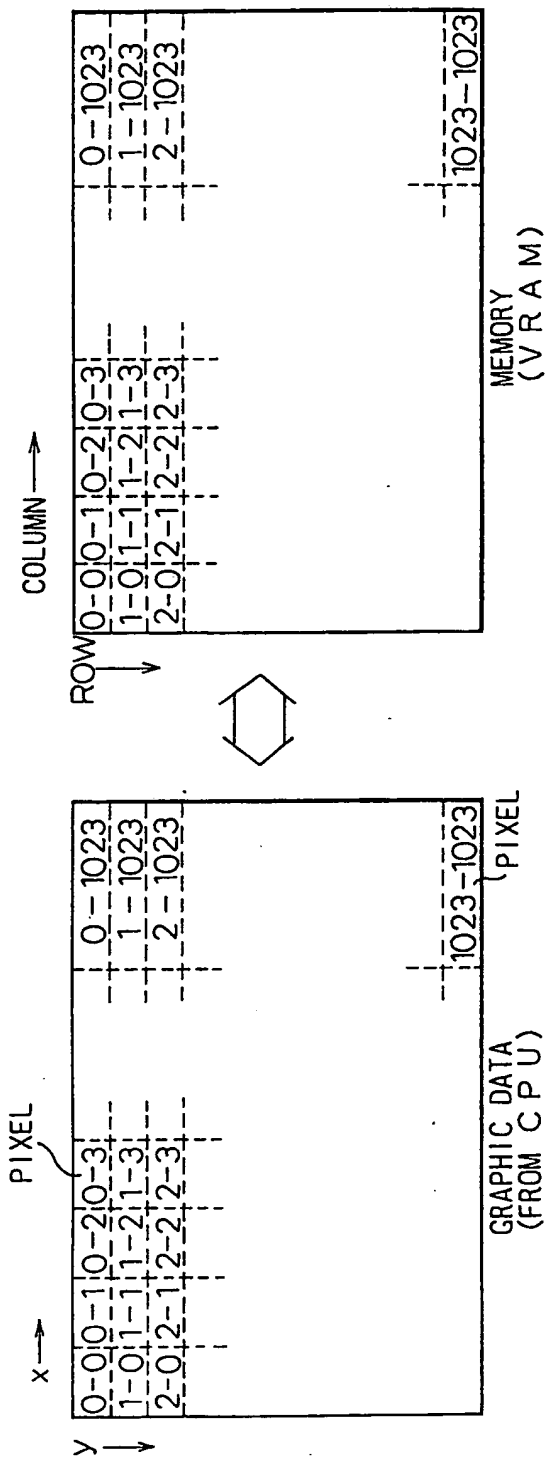

DRAWING CPU
VRAM
[TWO-PORT MEMORY]
VRAM
CONTROLLER
DAC
DISPLAY

Fig. 16


COLUMN
ROW
MEMORY
(V R A M)
PIXEL
GRAPHIC DATA
(FROM C P U)
PIXEL
x
y
0-0 0-1 0-2 0-3
1-0 1-1 1-2 1-3
2-0 2-1 2-2 2-3
0-1023
1-1023
2-1023
1023-1023

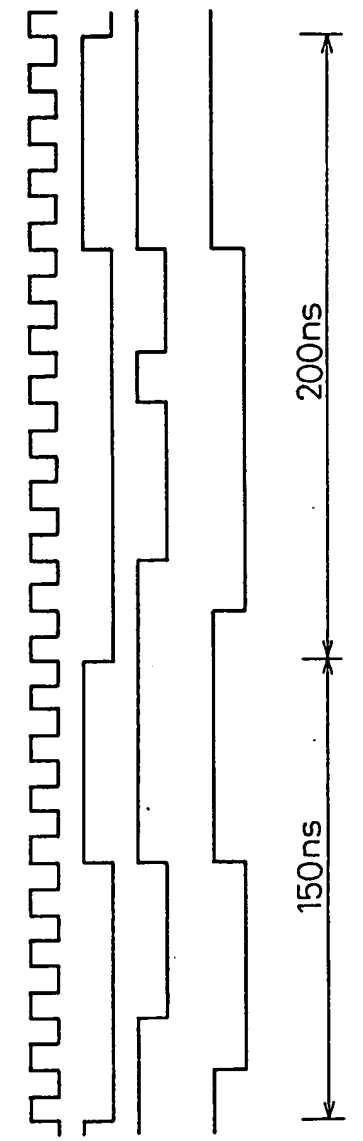


Fig.17

Fig.18A

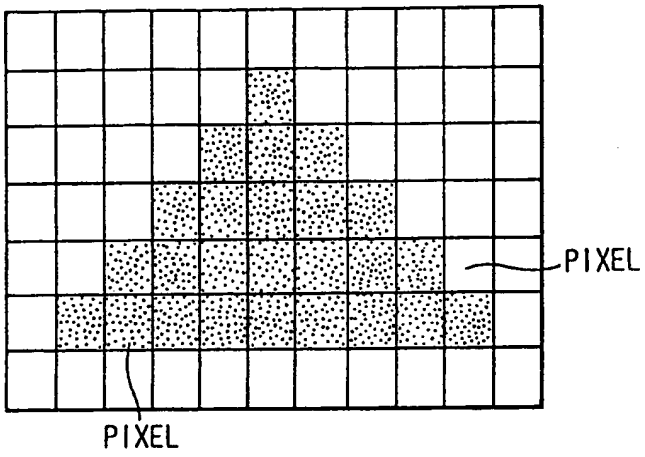


Fig.18B

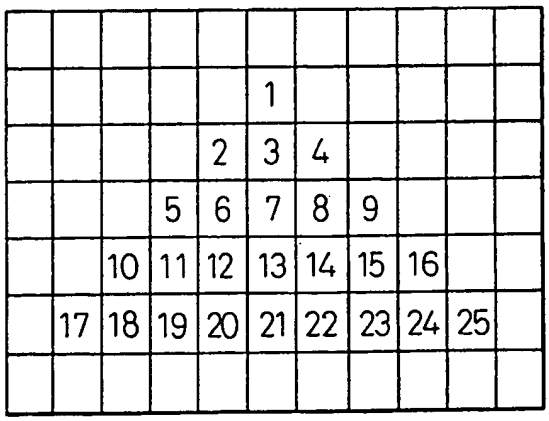


IMAGE PROCESSING SYSTEM

The present invention relates in one aspect to a system for accessing image memories which performs control for accessing image memories of the address multiplex mode and in another aspect to an image processing system which updates image data stored in image memories of the address multiplex mode and simultaneously displays the data on a display unit.

Computer graphic and other image processing systems are provided with image memories of the address multiplex mode which are accessed in accordance with addresses defined by row addresses and column addresses. These systems store image data in these image memories and display the stored image data on display units.

To make such image processing systems more practical, it is necessary for them to be able to perform high speed processing and to be able to be made at a low price and with a compact configuration.

A conventional image processing system carries a video RAM (VRAM) as an address multiplex mode image memory. It maps X-Y addresses of the image data and row-column addresses of the video RAM in one to one correspondence, stores the image data in the video RAM, and displays the stored image data by a display unit, i.e. is configured to update the image data stored in the video RAM while displaying the data by way of the display unit.

As explained in detail later with reference to the drawings, the system carries a two-port configuration video RAM able simultaneously to perform random access processing of the memory and sequential access processing for outputting data to the display unit, and mapping X-Y addresses of the image data and row-column addresses of the video RAM in one to one

correspondence. A drawing CPU uses the random access port of the video RAM to rewrite all or part of the image data stored in the video RAM, while a video RAM controller uses the sequential port of the video RAM to sequentially read out the image data stored in the video RAM. A digital-to-analog converter (DAC) converts the read out image data from digital signals to analog signals which are then displayed by the display unit.

With this related art, however, there was a problem in that high speed processing was not possible, as explained in detail later.

Also, with this related art, it was necessary to use a two-port memory video RAM, which is higher in price than a usual DRAM, so there was the problem that the price of the image processing system became higher. In addition, a two-port memory video RAM has a smaller memory capacity than a usual DRAM (having only one-quarter the memory capacity despite being the same size), so there was the problem that the image processing system could not be made compact.

Various aspects of the invention are exemplified by the attached claims from which it will be seen that one possibility is a new method for accessing an image memory which enables high speed processing when performing control for access of an image memory of the address multiplex mode and the provision of a new image processing system which enables high speed processing when updating and displaying by a display unit image data stored in the image memory of the address multiplex mode, is low in price, and can be realized compactly.

According to yet another aspect of the present invention, a system is provided with two multiple-bank image memories each having one picture's worth of capacity, assigns the same row address to each

rectangular region of the image data, is provided with two memory control units having address conversion means for converting the X-Y addresses of the image data to addresses of the image memories, switches the image memories in units of pictures repeatedly so that one control unit writes image data in one image memory and the other control unit reads image data from the other image memory, and is provided with a selection means for selecting either of the display image data output from the image memories and sending the same to the display unit.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, wherein:

Fig. 1 is a block diagram showing a first embodiment of the present invention;

Fig. 2 is a block diagram showing a second embodiment of the present invention;

Fig. 3 is a block diagram showing a third embodiment of the present invention;

Figs. 4A and 4B are diagrams explaining a first example of memory mapping according to the present invention;

Fig. 5 is a diagram explaining a second example of memory mapping according to the present invention;

Figs. 6A and 6B are diagrams explaining a third example of memory mapping according to the present invention;

Fig. 7 is a block diagram showing a special example of a first embodiment of the present invention;

Fig. 8 is a diagram explaining a synchronous DRAM;

Figs. 9A and 9B are diagrams of an example of memory mapping;

Fig. 10 is a block diagram showing a specific example of an address conversion means;

Fig. 11 is a block diagram showing a specific example of a second embodiment of the present invention;

Figs. 12A and 12B are diagrams of an example of memory mapping;

Fig. 13 is a block diagram showing a specific example of an address conversion means;

Fig. 14 is a block diagram showing a specific example of a third embodiment of the present invention;

Fig. 15 is a block diagram explaining the related art;

Fig. 16 is a block diagram explaining memory mapping in the related art;

Fig. 17 is a time chart of memory access of a video RAM; and

Figs. 18A and 18B are diagrams showing an example of the routine for access of image data.

Before describing exemplary embodiments of the present invention, the related art and the disadvantages therein will be described with reference to the related figures.

As explained above, a conventional image processing system carries a video RAM (VRAM) as an address multiplex mode image memory. It maps X-Y addresses of image data and row-column addresses of the video RAM, stores image data in the video RAM in one to one correspondence, and displays the stored image data by a display unit, i.e. updates the image data stored in the video RAM while displaying the data by means of the display unit.

That is, as shown in Fig. 15, it carries a two-port configuration video RAM able to simultaneously perform random access processing of the memory and sequential access processing for outputting data to the display unit and, as shown in Fig. 16, maps X-Y addresses of the image data and row-column addresses of the video RAM in one to one correspondence. The drawing CPU uses the random access port of the video RAM to rewrite all or part of

the image data stored in the video RAM, while the video RAM controller uses the sequential port of the video RAM to sequentially read out the image data stored in the video RAM. A digital-to-analog converter (DAC) converts the read out image data from digital signals to analog signals which are then displayed by the display unit.

In Fig. 16, the broken line blocks each show one pixel. For example, "2-3" shows a pixel of the coordinates (y,x) of (2,3). Each pixel has RGB and other data.

With this related art, however, there was the above-mentioned problem that high speed processing was not possible, as explained above.

That is, a video RAM (VRAM), like a usual DRAM, has the property of a slower access when changing the row address. Explaining this more specifically, if using a clock (CLK) frequency of 60 MHz, when writing data in the video RAM, it takes 150 ns to newly set the row address and then write the first pixel, then takes 50 ns (3 clocks) to write each succeeding pixel. Accordingly, it takes "(100 + 50 x n) ns" to access n number of pixels of the same row address. Figure 17 is a time chart of the accessing of a video RAM. Here, the RAS in the figure indicates a row-address strobe signal, CAS a column-address strobe signal, and WE a write enable signal.

As clear from Fig. 17, in the case of the same row address, it takes 150 ns to access one pixel (one signal CAS) and 200 ns to access two pixels (two signals CAS). Accordingly, when accessing with the same row address, it takes far less than double the time of accessing one pixel to access two pixels.

Explaining this more specifically, when drawing the triangular shape shown in Fig. 18A in the order of 1, 2, 3... shown in Fig. 18B, it takes 150 ns for writing the single pixel of the first stage, takes 250 ns for writing the three pixels of the second stage, takes 350 ns for writing the five pixels of the third stage, takes 450 ns for writing the seven pixels of the fourth stage, and takes 550 ns for writing the nine pixels of the fifth stage, so it takes a long total time of 1750 ns for the

processing.

For example, in image formation of a three-dimensional computer graphic, a polygon is formed by linking a large number of small triangles to draw a picture. Figure 18A shows a unit triangle for forming that polygon.

With this related art, it was necessary to use a two-port memory video RAM, which is higher in price than a usual DRAM, so there was the above problem that the price of the image processing system became higher. In addition, a two-port-memory video RAM has a smaller memory capacity than a usual DRAM (having only one-quarter the memory capacity despite being the same size), so there was the above problem that the image processing system could not be made compact.

The present embodiments can be designed to provide a new method for accessing an image memory which enables high speed processing when performing control for accessing an image memory of the address multiplex mode, and to provide a new image processing system which enables high speed processing when updating and displaying by a display unit image data stored in the image memory of the address multiplex mode, is low in price, and can be realized compactly.

Figures 1 to 3 show three embodiments of an image processing system 1 according to one aspect of the present invention.

The first embodiment of the image processing system 1 of the present invention shown in Fig. 1 is provided with a first image memory 10 of a multiple-bank configuration and address multiplex mode having a capacity able to store one picture's worth of data, a second image memory 11 of a multiple-bank configuration and address multiplex mode having a capacity able to store one picture's worth of data, a first memory control

unit 12 for executing access control processing for the first image memory 10, a second memory control unit 13 for executing access control processing for the second image memory 11, a selection means 14 for receiving the data outputs of the first and second image memories 10 and 11 and selecting one of the same to output display image data, a display unit 15 for displaying the display image data output by the selection means 14, a drawing calculation facility 16 for calculating and outputting the X-Y address/data values of drawing image data, and an output address calculation facility 17 for receiving as input a synchronization signal and calculating (calculating by incrementing X one by one and incrementing Y one by one in accordance with a raster scan) and outputting the X-Y address of the display image data.

The first memory control unit 12 is provided with an address conversion means 18 for converting an X-Y address of the input image data to a row-column address of the first image memory 10 and a memory mode determining means 19 for receiving the picture end signal produced from the synchronization signal and determining whether to write drawing image data in the first image memory 10 or read out display image data from the first image memory 10.

Further, the second memory control unit 13 is provided with an address conversion means 20 for converting an X-Y address of the input image data to a row-column address of the second image memory 20 and a memory mode determining means 21 for receiving the picture end signal produced from the synchronization signal and determining whether to write drawing image data in the second image memory 11 or read out display image data from the second image memory 11.

The second embodiment of the image processing system 1 of the present invention shown in Fig. 2 is provided with an image memory 30 of the address multiplex mode comprised of two banks, each bank having a capacity able

to store one picture's worth of data, a memory control unit 31 for executing access control processing for the image memory 30, a data adjusting means 32 for adjusting the image data output from the image memory 30 to produce display image data, a display unit 33 for displaying display image data generated by the data adjusting means 32, a drawing calculation facility 34 for calculating and outputting the X-Y address/data values of drawing image data, and an output address calculation facility 35 for receiving as input a synchronization signal and calculating and outputting the X-Y address of the display image data.

The memory control unit 31 is provided with an address conversion means 36 for converting the X-Y address of the input image data to the row-column address of the image memory 30, a bank mode determining means 37 for receiving the picture end signal produced from the synchronization signal and determining into which bank to write drawing image data and from which bank to read out display image data, and a time slice control means 38 for performing control to access, when a consecutive access to a different rectangular region (see 2 in Fig. 4) in the same bank is to be achieved, a rectangular region of another bank before the access of the former rectangular region.

The third embodiment of the image processing system 1 of the present invention shown in Fig. 3 is provided with a non-indicative information memory 40 of a multiple-bank configuration and address multiplex mode provided for storing image data other than display image data (non-indicative information) and having a capacity able to store one picture's worth of data, a video RAM 41 for storing the display image data, a first memory control unit 42 for executing access control processing for the non-indicative information image memory 40, a second memory control unit 43 for executing access control processing for the video RAM 41, a display unit

44 for displaying the display image data output by the video RAM 41, and a drawing calculation facility 45 for calculating and outputting the X-Y address/data values of the drawing image data.

Note that the "non-indicative information" includes for example depth information in a three-dimensional computer graphic.

The first memory control unit 42 is provided with an address conversion means 46 for converting an X-Y address of the input image data to a row-column address of the non-indicative information image memory 40.

The operation of the embodiments of the invention will be explained below.

In the first embodiment of the image processing system 1 shown in Fig. 1, when the memory mode determining means 19 receives a picture end signal, it decides to read display image data from the first image memory 10 if it had up until then decided to write drawing image data in the first image memory 10 and decides to write drawing image data in the first image memory 10 if it had up until then decided to read the display image data from the first image memory 10.

On the other hand, the memory mode determining means 21 decides to read display image data from the second image memory 11 if the memory mode determining means 19 decides on writing and decides to write drawing image data in the second image memory 11 if it decides on reading.

Receiving the decisions of the memory mode determining means 19 and 21, the address conversion means 18 and 20 receive the X-Y address output from the drawing calculation facility 16 when it is decided to write drawing image data in the image memories 10 and 11 and receive the X-Y address output from the output address calculation facility 17 when it is decided to read display image data from the image memories 10 and 11.

When receiving the X-Y address of the image data,

the address conversion means 18 and 20, as shown in Fig. 4A, assign the same row address of the image memories 10 and 11 to each rectangular region 2 of the image data and, as shown in Fig. 4B, assign column addresses of the image memories 10 and 11 to the rectangular regions 2 in accordance with the order of the raster scan. Further, as shown in Fig. 4A, they assign different banks (A, B) to adjoining rectangular regions 2. By this, they convert the received X-Y addresses to row-column addresses of the image memories 10 and 11.

The image memories 10 and 11 are accessed in accordance with the thus calculated row-column addresses, so the selecting means 14 selects the image memory 10 or 11 outputting display image data and displays display image data by the display unit 15.

By this configuration, when accessing the image memories 10 and 11, when the access is executed in the same rectangular region 2, the access can be performed without changing the row address and accordingly high speed access is possible. Note that if just this effect is desired, a single-bank configuration can be used and the same row address of the image memories 10 and 11 can be assigned to the rectangular region 2 of the image data as shown in Fig. 5.

When accessing the image memories 10 and 11, when the access spans different rectangular regions 2, since different banks are assigned to the adjoining rectangular regions of the same image data, by using an image memory such as a synchronous DRAM (SDRAM) which enables setting of a row address of another bank (B) during access, it becomes possible to set the row address of another bank (B) during access of any one bank (A). Accordingly, high speed access can be realized.

In this way, the first embodiment of the image processing system shown in Fig. 1 enables high speed accessing of the image memories 10 and 11. The image processing system 1 can update and display by the display

unit 15 drawing image data without use of an expensive, large sized video RAM.

In the second embodiment of the image processing system 1 shown in Fig. 2, when the bank mode determining means 37 receives the picture end signal, when there are two banks, that is, the bank A and the bank B, the system decides to read display image data from the bank A when having decided up to then to write drawing image data in the bank A and decides to write the drawing image data in the bank B when having decided up to then to read the display image data from the bank B.

On the other hand, the time slice control means 38 decides in accordance with the later mentioned algorithm whether to receive the X-Y address output by the drawing calculation facility 34 or to receive the X-Y address output by the output address calculation facility 35. When deciding to receive the X-Y address output from the drawing calculation facility 34, it instructs the output address calculation facility 35 to temporarily stop the transmission of the X-Y address, while when deciding to receive the X-Y address output from the output address calculation facility 35, it instructs the drawing calculation facility 34 to temporarily stop the transmission of the X-Y address.

When receiving the X-Y address of either of drawing image data or display image data in accordance with this control processing of the time slice control means 38, the address conversion means 36 assigns the same row address of the image memory 30 to each rectangular region 2 of the image data as shown in Fig. 6A and assigns column addresses of the image memory 30 to the rectangular regions 2 in accordance with the raster scan as shown in Fig. 6B. Further, it assigns the same bank to each rectangular region 2 of the same image data and thereby converts the received X-Y address to the row-column address of the image memory 30.

When executing such address conversion processing,

the time slice control means 38 performs control to access, when a consecutive access to a different rectangular region in the same bank (A) is to be achieved, a rectangular region of another bank (B) before the access of the former rectangular region, so as to decide whether to receive the X-Y address output from the drawing calculation facility 34 or to receive the X-Y address output from the output address calculation facility 35.

That is, when receiving the X-Y address output from the drawing calculation facility 34, when shifting to a rectangular region 2 with a different X-Y address, it is decided to temporarily stop the reception of the X-Y address and then receive the X-Y address output from the output address calculation facility 35. On the other hand, when receiving the X-Y address output from the output address calculation facility 35, when shifting to a rectangular region 2 with a different X-Y address, it is decided to temporarily stop the reception of the X-Y address and then receive the X-Y address output from the drawing calculation facility 34.

The writing of drawing image data (from the CPU) and the reading of display image data (to the display) are alternately performed at the border of the rectangular regions 2 in accordance with the row-column address calculated in that way. That is, display image data output from the image memory 30 is not consecutively output, but is output sandwiched between adjoining drawing image data, so the data adjusting means 32 extracts display image data output from the image memory 30, converts them to consecutive data, and displays the result by the display unit 33.

By this configuration, when accessing the image memory 30, when the access is in the same rectangular region 2, the access can be performed without changing the row address and therefore high speed access can be realized.

Further, when accessing the image memory 30 and when the access spans different rectangular regions 2, since two banks are switched by a time division mode at the border of the rectangular regions (A->B or B->A), by using an image memory such as a synchronous DRAM (SDRAM) which enables setting of a row address of another bank during access, it becomes possible to set the row address of the other bank (B) during access of any one bank (A). Accordingly, high speed access can be realized.

The second embodiment of the image processing system 1 shown in Fig. 2 enables high speed access of the image memory 30. The image processing system 1 can update and display on the display unit 33 drawing image data without use of an expensive large sized video RAM (VRAM).

In the third embodiment of the image processing system 1 shown in Fig. 3, like with the related art, a video RAM 41 is provided for updating and displaying on a display unit 44 the image data. Here, the non-indicative information such as the depth information of drawing image data output from the drawing calculation facility 45 is received by the first memory control unit 42.

When receiving an X-Y address of the non-indicative information, the address conversion means 46, as shown in Fig. 4A, assigns the same row address of the non-indicative information memory 40 to each rectangular region 2 of the image data and, as shown in Fig. 4B, assigns column addresses of the non-indicative information memory 40 to the rectangular regions 2 in accordance with the raster scan. Further, it assigns different banks (A, B) to the adjoining rectangular regions 2. By this, it converts the received X-Y addresses to row-column addresses of the non-indicative information memory 40.

The non-indicative information memory 40 is accessed in accordance with the thus calculated row-column address, but this access can be realized at a high speed for the same reason as explained with reference to Fig. 1.

In this way, the third embodiment of the image processing system shown in Fig. 3 writes and reads the non-indicative information of drawing image data in and from the non-indicative information memory 40 at a high speed.

The present invention will now be explained in further detail using specific examples.

Figure 7 shows a specific example of the image processing system 1 of the present invention shown in Fig. 1. In the figure, parts the same as those explained with reference to Fig. 1 are shown by the same references.

Reference numeral 100 is a digital signal processor. This processor 100 includes a first memory control unit 12, a second memory control unit 13, a drawing calculation facility 16, and an output address calculation facility 17. Reference numeral 10a is a first synchronous DRAM (SDRAM) corresponding to the first image memory 10, 11a is a second synchronous DRAM (SDRAM) corresponding to the second image memory 11, and 14a is a selector corresponding to the selection means 14. Reference numeral 22 is a digital-to-analog converter, which converts display image data output by the selector 14a from digital to analog signals, and 23 is a synchronization signal generating facility, which produces synchronization signals.

Before explaining the specific example, an explanation will be made of a synchronous DRAM (SDRAM).

A synchronous DRAM is comprised of two banks (A and B) and although is slow in accesses involving changes in row addresses and accesses involving changes in read and write operations, it extremely fast in read accesses and write accesses of several words length of the same row address. Further, it is able to change the row address of one bank (B or A) while it is accessing another bank (A or B). Therefore, it is also possible to increase the speed of access to different row addresses. Further, it

automatically accesses column addresses by successively incrementing by one the designated column address.

For example, as shown in Fig. 8, if a row address a and column address a1 are set for a bank A, write access is performed on the successively incremented four column addresses (1 -> 2 -> 3 -> 4). During this time, it is possible to set the row address b of the bank B. When the column address a2 of the bank A is next set, write access is performed for the successively incremented four column addresses. Next, when the column address b1 of the bank B is set, write access is performed for the successively incremented four column addresses. In this way, it is possible to change the row addresses of one bank while accessing another bank and, further, it is possible to automatically access the column addresses successively incremented from the designated column address.

Next, an explanation will be made of the specific example of Fig. 7.

In the specific example of Fig. 7, as explained with reference to Fig. 1, one of the synchronous DRAMs 10a and 11a is used for accessing from the drawing calculation facility 16 and the other of the synchronous DRAMs 10a and 11a is used for accessing from the output address calculation facility 17. The roles of these two synchronous DRAMs 10a and 11a are switched when the drawing calculation facility 16 finishes drawing one picture. By this, processing is performed to write drawing image data in the synchronous DRAMs 10a and 11a provided as double buffers and to read out display image data and display the same by the display unit 15.

The synchronous DRAMs 10a and 11a are supposed to have capacities enough to store one picture's worth of data, so for example when one picture is comprised of 2048 x 1024 pixels, they are given capacities of 2048 x 1024 pixels with their two banks.

The address conversion means 18 and 19 provided in the first and second memory control units 12 and 13,

which cooperate with the synchronous DRAMs 10a and 11a, as explained in Fig. 4A and Fig. 4B, assign the same row addresses of the synchronous DRAMs 10a and 11a to the rectangular regions 2 of the image data and assign the column addresses of the synchronous DRAMs 10a and 11a to the rectangular regions 2 in accordance with the raster scan. Further, they assign different banks to the adjoining rectangular regions 2. By this, processing is performed to convert an X-Y address received to a row-column address of the synchronous DRAMs 10a and 11a.

Figures 9A and 9B show an example of this memory mapping. In this example, a rectangular region 2 is formed by 32 x 32 pixels.

This memory mapping is specifically realized in accordance with the following:

$$R.A = INT\ (y/32) * 32 + INT\ (x/64)$$

$$B.A = mod_2\ (mod_2\ (INT\ (x/32)) + mod_2\ (INT\ (y/32)))$$

$$C.A = mod_{32}(x) + mod_{32}\ (y) * 32 \qquad (1)$$

Here, "R.A" in equation (1) means the row address, "B.A" the bank address, and "C.A" the column address. "B.A = 0" indicates the bank A and "B.A = 1" indicates the bank B.

Further INT means an integer and * indicates a multiplication operation.

Figure 10 illustrates an example of the hardware configuration of the address conversion means 18 or 19 (both having the same configuration) for realizing equation (1). Here, X(0) indicates the least significant bit of the X address, X(10) the most significant bit of the X address, Y(0) indicates the least significant bit of the Y address, Y(9) the most significant bit of the Y address, ROW(0) indicates the least significant bit of the row address, ROW(9) the most significant bit of the row address, and COLUMN(0) indicates the least significant bit of the column address, and COLUMN(9) the most significant bit of the column address.

By this hardware configuration, when for example receiving an X-Y address of the image data of "X=64,

Y=32", the address conversion means 18 (19) performs address conversion processing for realizing the memory mapping shown in Figs. 9A and 9B in accordance with "X=00001000000, Y=000100000" to give "row address = 0000100001, column address = 0000000000, and bank address = 1", that is, "row address = 33, column address = 0, bank address = B".

The correspondence between the above equation (1) and the configuration of Fig. 10 is shown by <1>, <2>... <9> shown in Fig. 10. Here, <1>, <2>... <9> have the following meanings:

<1>	INT (y/32)	R.A
<2>	*32	R.A
<3>	INT (x/64)	R.A
<4>	mod_2	B.A
<5>	mod_2 (INT (x/32))	B.A
<6>	mod_2 (INT (y/32))	B.A
<7>	mod_2 (x)	C.A
<8>	mod_{32} (y)	C.A
<9>	*32	C.A

The synchronous DRAMs 10a and 11a are accessed in accordance with the row-column address calculated by this address conversion processing. Usually, however, the image data drawn by computer graphics etc. have a localized property, so often fit in the same rectangular region. At such times, by allocating the same row address in each rectangular region 2, it is possible to realize write access of the synchronous DRAMs 10a and 11a without changing the row address. An example of the above localization is shown by the triangular shapes in the rectangular region 2' in Fig. 4A.

When outputting display image data, the inside of the same rectangular region 2 is scanned in the horizontal direction, so by allocating the same row address to the inside of the rectangular region 2 (Fig. 4A), read access of the synchronous DRAMs 10a and 11a can be realized without changing the row address in the

rectangular region 2. Further, since the column addresses of the synchronous DRAMs 10a and 11a are assigned in accordance with the order of raster scanning to the rectangular regions (Fig. 4B), extremely high speed access is realized in accordance with the above-mentioned column address consecutive access function of the synchronous DRAMs 10a and 11a.

Further, since different banks are assigned to adjoining rectangular regions 2 of the same image data, even when the drawing image data spans adjoining rectangular regions (see 3 in Fig. 4A) and the write access shifts to the adjoining rectangular region or the read access shifts to the adjoining rectangular region in accordance with the raster scan, it is possible to set the row address of the other bank during the access in accordance with the row address setting function of the synchronous DRAMs 10a and 11a, so de facto consecutive access is realized.

On the other hand, the selector 14a selects the synchronous DRAM 10a or 11a which is outputting display image data in accordance with a picture end signal produced from the synchronization signal, since the display image data is output from one of the synchronous DRAMs 10a and 11a which are switched with each picture. The output display image data is output to the digital-to-analog converter (DAC) 22. Receiving this output, the digital-to-analog converter 22 converts the display image data output by the selector 14a from digital signals to analog signals which are then displayed by the display unit 15.

In this way, the image processing system 1 shown in Fig. 7 is provided with two single-port configuration synchronous DRAMs 10a and 11a and switches between the synchronous DRAM 10a (11a) for writing of drawing image data and the synchronous DRAM 11a (10a) for reading of display image data to enable updating and displaying on the display unit 15 of the drawing image data. By this,

the image processing system 1 can update and display on the display unit 15 the drawing image data without use of an expensive large sized video RAM (VRAM).

Figure 11 shows a specific example of the second embodiment of the image processing system 1 of the present invention shown in Fig. 2. In the figure, parts the same as those explained with reference to Fig. 2 are shown by the same references.

Reference numeral 100 is a digital signal processor. This processor 100 includes a memory control unit 31, a drawing calculation facility 34, and an output address calculation facility 35. Reference numeral 30a is a synchronous DRAM (SDRAM) corresponding to the image memory 30, and 32a is a rate conversion buffer corresponding to the data adjusting means 32. Reference numeral 39 is a digital-to-analog converter, which converts display image data produced by the rate conversion buffer 32a from digital to analog signals, and 40 is a synchronization signal generating facility, which produces synchronization signals.

In the specific example of Fig. 11, as explained with reference to Fig. 2, the synchronous DRAM 30a has two banks, that is, the banks A and B. One of the banks A or B is used for access from the drawing calculation facility 34, while the other of the banks A or B is used for access from the output address calculation facility 35. The roles of these two banks A and B are switched at the stage when the drawing calculation facility 34 finishes drawing one picture. In this way, drawing image data is written in the two banks A and B of the synchronous DRAM 30a provided as a double buffer and the display image data are read out and displayed by the display unit 33.

The banks A and B of the synchronous DRAM 30a are supposed to have capacities enough to store one picture's worth of data, so for example when one picture is comprised of 2048 x 1024 pixels, the banks A and B are

given capacities of 2048 x 1024 pixels.

The address conversion means 36 (Fig. 2) provided in the memory control unit 31, which cooperates with the synchronous DRAM 30a, as explained in Fig. 2, assigns the same row address of the synchronous DRAM 30 to the each rectangular region 2 of the image data and assigns the column addresses of the synchronous DRAM 30a to each rectangular region 2 in accordance with the raster scan. Further, it assigns the same bank to each rectangular region 2 of the same image data. By this, processing is performed to convert an X-Y address received to a row-column address of the synchronous DRAM 30a.

Figures 12A and 12B show an example of this memory mapping. In this example, a rectangular region 2 is formed by 32 x 32 pixels.

This memory mapping is specifically realized in accordance with the following:

$$R.A = INT\ (y/32) * 64 + INT\ (x/32)$$

$$C.A = mod_{32}\ (x) + mod_{32}\ (y) * 32 \qquad (2)$$

Here, "R.A" in equation (2) means the row address, and "C.A" the column address. When accessing the bank A, the least significant bit of the Y address is set to "0", while when accessing the bank B, the most significant bit of the Y address is set to "1".

Figure 13 illustrates an example of the hardware configuration of the address conversion means 36 for realizing equation (2). Here, X(0) indicates the least significant bit of the X address, X(10) the most significant bit of the X address, Y(0) indicates the least significant bit of the Y address, Y(9) the most significant bit of the Y address, ROW(0) indicates the least significant bit of the row address, ROW(10) the most significant bit of the row address, and COLUMN(0) indicates the least significant bit of the column address, and COLUMN(9) the most significant bit of the column address.

By this hardware configuration, when for example

receiving an X-Y address of the image data of "X=32, Y=32", when accessing the bank A, the address conversion means 36 performs address conversion processing for realizing the memory mapping shown in Figs. 12A and 12B in accordance with "X=00000100000, Y=0000100000" to give "row address = 00001000001, column address = 0000000000, and bank address = 0", that is, "row address = 65, column address = 0, bank address = A".

The correspondence between the above equation (2) and the configuration of Fig. 13 is shown by <1>, <2>... <6> shown in Fig. 13. Here, <1>, <2>... <6> have the following meanings:

<1>	INT (y/32)	R.A
<2>	*64	R.A
<3>	INT (x/64)	R.A
<4>	mod_2 (x)	C.A
<5>	mod_{32} (y)	C.A
<6>	*32	C.A

The synchronous DRAM 30a is accessed in accordance with the row-column address calculated by this address conversion processing. Usually, however, the image data drawn by computer graphics etc. have a localized property (see triangular shapes in the region 2' in Fig. 4A), so often fit in the same rectangular region 2. At such times, by allocating the same row address to the rectangular region 2, it is possible to realize write access of the synchronous DRAM 30a without changing the row address.

When outputting display image data, the inside of the same rectangular region 2 is scanned in the horizontal direction, so by allocating the same row address to the inside of the rectangular region 2, read access of the synchronous DRAM 30a can be realized without changing the row address in the rectangular regions 2. Further, since the column addresses of the synchronous DRAM 30a are assigned in accordance with the order of raster scanning to the rectangular regions,

extremely high speed access is realized in accordance with the above-mentioned column address consecutive access function of the synchronous DRAM 30a.

Further, when accessing the synchronous DRAM 30a, when the access spans different rectangular regions (see 3 in Fig. 4A), since the two banks are switched in a time division mode at the border of the rectangular regions 2, even if drawing image data does not fit in the same rectangular region and crosses to the adjoining rectangular region and thereby the write access shifts to the adjoining rectangular region or the read access shifts to the adjoining rectangular region in accordance with the raster scan, it is possible to set the row address of the other bank during the access in accordance with the row address setting function of the synchronous DRAM 30a, so de facto consecutive access is realized.

In accordance with the specific example of Fig. 11, the writing of drawing image data and the reading of display image data are alternately performed by a time division mode, so the display image data output from the synchronous DRAM 30a is not consecutively output, but is output sandwiched between the adjoining drawing image data.

Therefore, the rate conversion buffer 32a extracts display image data output from the synchronous DRAM 30a and converts it to consecutive data for display by the display unit 33. For example, it has a capacity of two lines' worth of data, converts display image data output from the synchronous DRAM 30a to consecutive data, during the scan of one line of the display unit 33, stores one line's worth in another buffer, and outputs this in accordance with the display frequency when scanning the next line.

With such a processing and configuration, in the specific example of Fig. 7, when the memory access speed is slower than the display frequency, it is not possible to output the correct image data. Further, when the

memory access speed is faster than the display frequency, it is not possible to make full use of the memory performance. As opposed to this, with the configuration of Fig. 11, it is possible to freely set the rate of display output access relative to the full memory access, so it is possible to obtain the maximum drawing performance.

The third embodiment of the image processing system 1 shown in Fig. 11 is provided with a two-bank configuration synchronous DRAM 30a having a single port and switches the bank for writing of drawing image data and the bank for reading display image data in units of pictures so as to enable updating and displaying on the display unit 33 of the drawing image data. By this, the image processing system 1 can update and display on the display unit 33 drawing image data without use of an expensive large sized video RAM (VRAM).

Figure 14 illustrates a specific example of the third embodiment of the image processing system 1 of the present invention shown in Fig. 3. In the figure, parts the same as those explained with reference to Fig. 3 are shown by the same references.

Reference numeral 100 is a digital signal processor. This processor 100 includes a first memory control unit 42, a second memory control unit 43, and a drawing calculation facility 45. Reference numeral 40a is a synchronous DRAM corresponding to the non-indicative information image memory 40, 47 is a digital-to-analog converter, which converts display image data output by the video RAM 41 from digital to analog signals, and 48 is a synchronization signal generating facility, which produces synchronization signals.

In the image processing system 1 of the third embodiment, like with the related art, inclusion of a video RAM 41 enables the image data to be updated and at the same time displayed on the display unit 44, but the depth information and the control information, which are

never output to the display unit 44, are stored in the synchronous DRAM 40a.

That is, in the case of the configuration of Fig. 7, the synchronous DRAM 10a or 11a which is outputting to the display unit 15 cannot be accessed from the drawing calculation facility 16, so to solve this, the image plane requiring display output access is stored in the two-port configuration video RAM 41 and the plane not requiring display output access is stored in the synchronous DRAM 40a. Note that the image plane in many cases need only be written, but the depth information etc. in most cases is first read and then written. When two sets of image data are superposed three-dimensionally, which set of image data is in front is calculated by reading the data and the resultant data is written once again.

When receiving an X-Y address of such non-indicative information from the drawing calculation facility 45, the address conversion means 46 executes the same type of address conversion processing as with the address conversion means 18 and 19 of the configuration of Fig. 7, and as a result the synchronous DRAM 40a is accessed at a high speed in accordance with the row-column address sought.

In this way, the image processing system 1 shown in Fig. 14 can write the non-indicative information of drawing image data at a high speed in the synchronous DRAM 40a and can read it at a high speed from the synchronous DRAM 40a.

While the invention has been described by reference to the specific embodiments chosen for purposes of illustration, it should be apparent that numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention. For example, in the examples, disclosure was made of the case of use of a synchronous DRAM, but the invention is not limited to this.

In the final analysis, if the triangular shape shown in Fig. 18A is written by 25 pixels in accordance with the order shown in Fig. 18B, then, as mentioned above, according to the related art, 1750 ns would be required until the completion of the write operation. If the triangular shape fits in the same rectangular region 2, however, the present invention enables this to be shortened to 1350 ns, even with the same access speed as a video RAM, since there is no need to change the row address. Note that in this case, if use is made of a synchronous DRAM, continuous access becomes possible even when the triangular shape does not fit into the same rectangular region 2 and one access can be one clock (16.7 ns), so the time required for access can be greatly shortened to "16.7 x number of pixels = 16.7 x 25 = 418 ns".

As explained above, according to the present invention, it becomes possible to access address multiplex mode image memories at a high speed. Further, it becomes possible to update and display on a display unit image data stored in address multiplex mode image memories while realizing high speed processing and without use of high priced, large sized video RAMs.

CLAIMS

1. A method for accessing image data by access to an image memory of an address multiplex mode,

said method for accessing image data being characterized by

assigning the same row address of the image memory to each rectangular region of the image data,

converting an X-Y address of the image data to a storage address of the image memory by an address conversion means, and

accessing the image memory in accordance with the storage address converted by the address conversion means.

2. A method for accessing image data as set forth in claim 1, wherein said address conversion means is operative to assign column addresses of the image memory to the rectangular regions of the image data in accordance with the order of the raster scan.

3. A method for accessing image data as set forth in claim 1 or 2, wherein when said image memory is comprised of two or more banks, said address conversion means is operative to assign different banks to adjoining rectangular regions of the same image data.

4. A method for accessing image data as set forth in claim 1 or 2, wherein

when said image memory is comprised of two or more banks, said address conversion means is operative to assign the same bank to each rectangular region of the same image data and

when a consecutive access to a different rectangular region in the same bank occurs, control is performed by a time slice control means to access the rectangular region of the other bank before that access.

5. An image processing system which performs processing so as to update and display on a display unit image data stored in an image memory of the address

multiplex mode,

said image processing system being provided with,

as the image memory of the address multiplex mode, two multiple-bank configuration image memories each having one picture's worth of capacity,

two memory control units each provided with an address conversion means for performing processing for assigning different banks to the adjoining rectangular regions of the same image data when the image memories are comprised of two or more banks and calculating the storage addresses of the image memories in accordance with the address conversion means,

wherein the image memories are switched in units of pictures so that one of said memory control units writes drawing image data in one of said image memories and the other memory control unit reads display image data from the other image memory, and

a selection means for receiving as input the data outputs of the two image memories, selecting the image memory which is outputting the display image data, and sending the display image data to the display unit.

6. An image processing system which performs processing so as to update and display on a display unit image data stored in an image memory of the address multiplex mode,

said image processing system being provided with,

as the image memory of the address multiplex mode, one image memory comprised of two banks, each bank having one picture's worth of storage capacity,

a memory control unit provided with an address conversion means for performing processing for assigning the same bank to each rectangular region of the same image data and a time slice control means for performing control so that when a consecutive access to a different rectangular region in the same bank occurs, the

rectangular region of another bank is accessed before that access, calculating the storage addresses of the image memories in accordance with the address conversion means, and switching the accessed banks in accordance with the time slice control means,

wherein the memory control unit repeatedly switches the banks in units of pictures so as to write drawing image data in one bank and read display image data from the other bank, and

a data adjusting means for extracting the display image data being read out at set time intervals by the time slice control means, converting the display image data to consecutive data, and sending the same to the display unit.

7. An image processing system as set forth in claim 5 or 6, wherein said image memory is comprised using a two-bank configuration synchronous DRAM.

8. An image processing system which performs processing so as to update and display on a display unit image data stored in an image memory of the address multiplex mode,

said image processing system being provided with,

as the image memory of the address multiplex mode, separate from a video RAM storing display image data, a non-indicative information image memory of a multiple-bank configuration having one picture's worth of storage capacity for storing image data other than the display image data and

a memory control unit provided with an address conversion means for performing processing for assigning different banks to adjoining rectangular regions of the same image data when the image memory is comprised of two or more banks, calculating storage addresses of the non-indicative information image memory in accordance with the address conversion means, and performing processing for accessing the non-indicative information image

memory.

9. An image processing system as set forth in claim 8, wherein the non-indicative information image memory is comprised using a two-bank configuration synchronous DRAM.

10. An accessing method or an image processing system according to any one of the examples substantially as hereinbefore described with reference to Figures 1 to 14 of the accompanying drawings.

The Patent Office

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Application No: GB 9501802.4 **Examiner:** R.F.KING
Claims searched: **Date of search:** 15 March 1995

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.N): H4F[FESA,FESG,FESK,FESX];
H4T[TBAD,TCGA,TCGD,TCGG,TCGK,TCGX]

Int Cl (Ed.6): G06T 1/60

Other: ONLINE DATABASE: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X A	GB2 257 599 A	See whole document	1 1,5,6,8
X A	GB2 208 095 A	See abstract	1 1,5,6,8

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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The Patent Office

1st further Search

31

Application No: GB 9501802.4 **Examiner:** R F KING
Claims searched: 5 and 7 **Date of search:** 17 August 1995

Patents Act 1977
Further Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.N): H4T[TBAD, TBEC]

Int Cl (Ed.6): G06T 1/20, 1/60

Other: Online Database: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2 264 616 A	[Apple.] See references to use of VRAM in plural bank configuration.	5
X	US 5,239,512	[US Philips] See Figs. 2, 3 and abstract, division of image into blocks and mapping of addresses into RAM.	5
X	US 4,912,771	[Canon] See use of two memories and switching of read/write use.	5

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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The Patent Office

2nd further Search

32

Application No: GB 9501802.4 **Examiner:** R F KING
Claims searched: 6 and 7 **Date of search:** 17 August 1995

Patents Act 1977
Further Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.N): H4T[TBAD]

Int Cl (Ed.6): G06T 1/60

Other: Online Database: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2 264 616 A	[Apple Comp.] See abstract	6
A	GB 2 208 095 A	[Racal Defence] See abstract	6
A	US 5,239,512	[US. Philips Corp.] See abstract	6

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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The Patent Office

3rd further search

33

Application No: GB 9501802.4 **Examiner:** R F KING
Claims searched: 8 and 9 **Date of search:** 17 August 1995

Patents Act 1977
Further Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.N): H4T[TBAD, TBEC]

Int Cl (Ed.6): G06T 1/20, 1/60

Other: Online Database: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	None	8

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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